FAIRCHILD SEMICONDUCTOR™

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# MM74HC4060
# 14 Stage Binary Counter

## General Description

The MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4060 is a 14-stage counter, which device increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The MM74HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to $V_{CC}$ and ground.

## Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

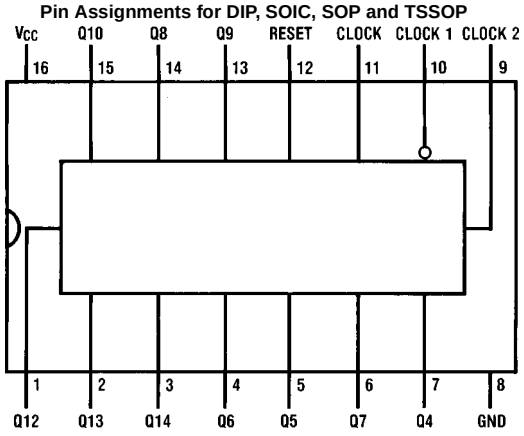
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC4060M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow |
| MM74HC4060SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC4060MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC4060N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

## Connection Diagram

**Pin Assignments for DIP, SOIC, SOP and TSSOP**




**Top View**

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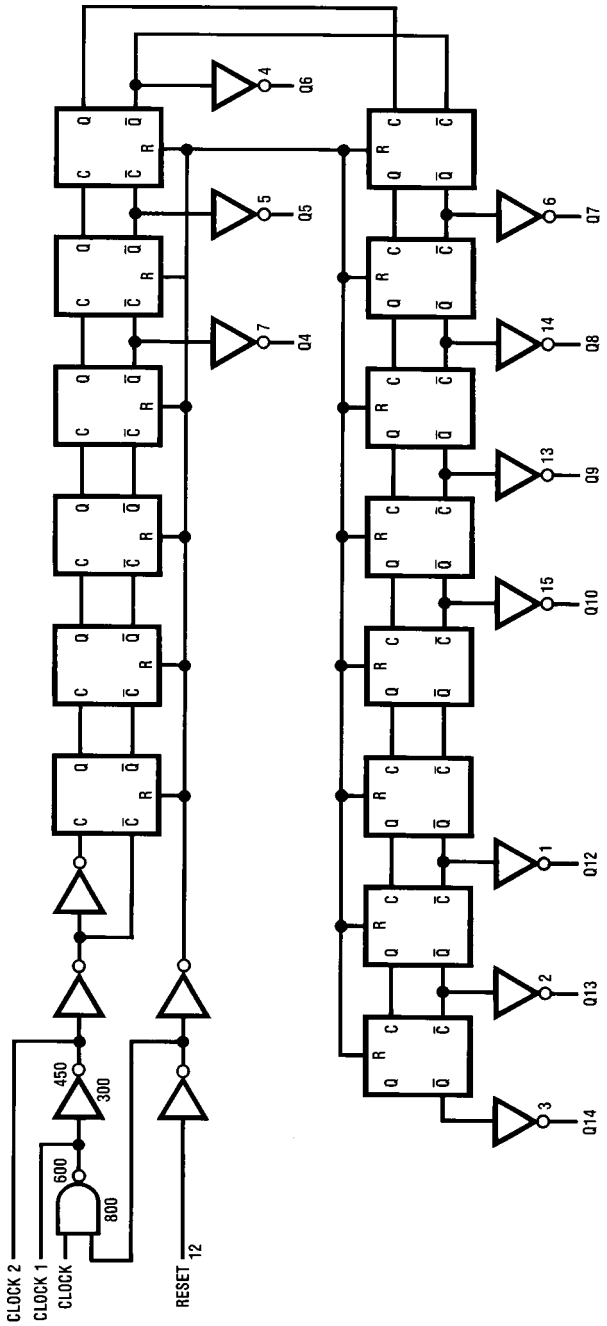
## Logic Diagram



## Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{CD}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage | | | |
| ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |
| Input Rise or Fall Times | | | |
| ($t_r$, $t_f$) $V_{CC}$ = 2.0V | | 1000 | ns |
| $V_{CC}$ = 4.5V | | 500 | ns |
| $V_{CC}$ = 6.0V | | 400 | ns |

**Note 1:** Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH | | | 2.0V | | 1.5 | 1.5 | 1.5 | V |
| | Level Voltage | | | 4.5V | | 3.15 | 3.15 | 3.15 | V |
| | (Not Applicable to Pins 9 & 10) | | | 6.0V | | 4.2 | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum LOW Level | | | 2.0V | | 0.5 | 0.5 | 0.5 | V |
| | Input Voltage | | | 4.5V | | 1.35 | 1.35 | 1.35 | V |
| | (Not Applicable to Pins 9 & 10) | | | 6.0V | | 1.8 | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum HIGH Level | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | Output Voltage | | $\|I_{OUT}\| \leq 20\ \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V |
| | | Except Pins | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | 9 & 10 | $\|I_{OUT}\| \leq 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | | $\|I_{OUT}\| \leq 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| | | Pins | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 3.98 | 3.84 | 3.7 | V |
| | | 9 & 10 | $\|I_{OUT}\| = 0.4$ mA | | | 5.48 | 5.34 | 5.2 | V |
| | | | $\|I_{OUT}\| = 0.52$ mA | | | | | | |
| $V_{OL}$ | Maximum LOW Level | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | Output Voltage | | $\|I_{OUT}\| \leq 20\ \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | Except Pins | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | 9 & 10 | $\|I_{OUT}\| \leq 4.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | | $\|I_{OUT}\| \leq 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | Pins | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.26 | 0.33 | 0.4 | V |
| | | 9 & 10 | $\|I_{OUT}\| = 0.4$ mA | | | 0.26 | 0.33 | 0.4 | V |
| | | | $\|I_{OUT}\| = 0.52$ mA | | | | | | |
| $I_{IN}$ | Maximum Input Current | | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ | Maximum Quiescent | | $V_{IN}$ = $V_{CC}$or GND | | | | | | |
| | Supply Current | | $I_{OUT}$ = 0 µA | 6.0V | | 8.0 | 80 | 160 | µA |

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $t_r$ = $t_f$ = 6 ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | 30 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay to $Q_4$ | (Note 5) | 40 | 20 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay to any Q | | 16 | 40 | ns |
| $t_{REM}$ | Minimum Reset Removal Time | | 10 | 20 | ns |
| $t_W$ | Minimum Pulse Width | | 10 | 16 | ns |

## AC Electrical Characteristics

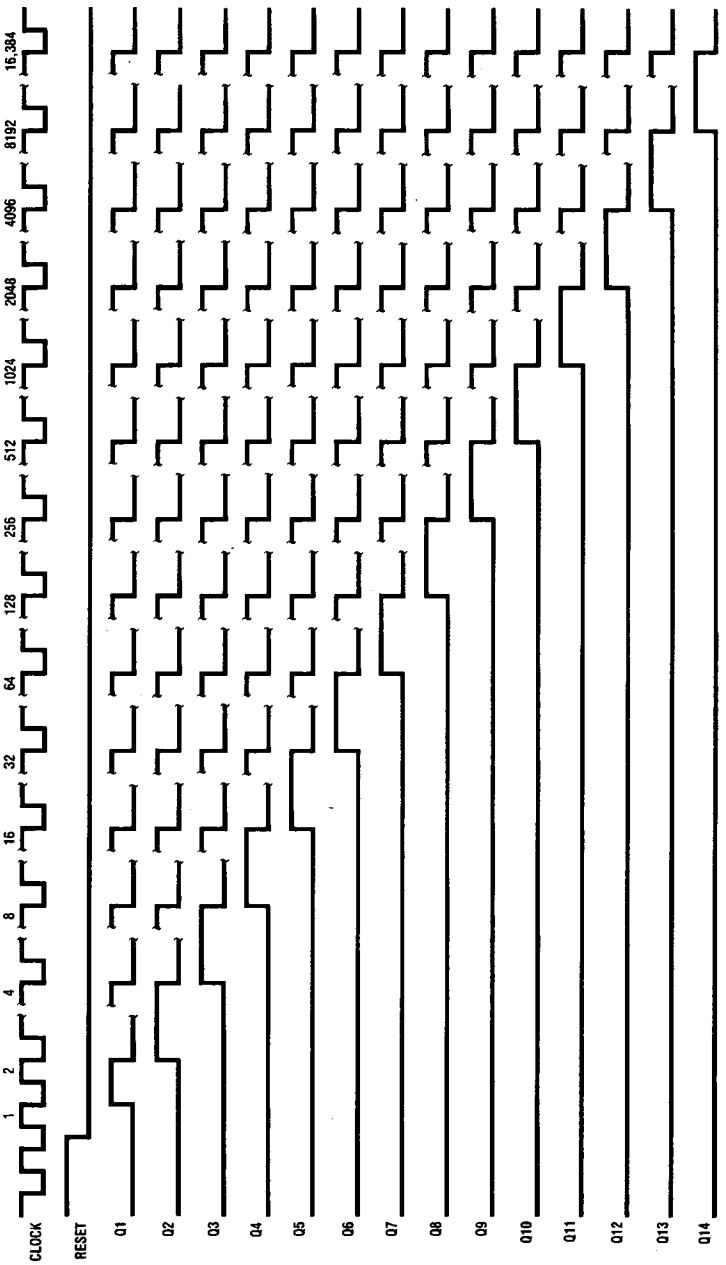
$V_{CC}$ = 2.0V to 6.0V, $C_L$ = 50 pF, $t_r$ = $t_f$ = 6 ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $f_{MAX}$ | Maximum Operating Frequency | | 2.0V | | 6 | 5 | 4 | MHz |
| | | | 4.5V | | 30 | 24 | 20 | MHz |
| | | | 6.0V | | 35 | 28 | 24 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay Clock to $Q_4$ | | 2.0V | 120 | 380 | 475 | 171 | ns |
| | | | 4.5V | 42 | 76 | 95 | 114 | ns |
| | | | 6.0V | 35 | 65 | 81 | 97 | ns |
| $t_{PHL}$ | Maximum Propagation Delay Reset to any Q | | 2.0V | 72 | 240 | 302 | 358 | ns |
| | | | 4.5V | 24 | 48 | 60 | 72 | ns |
| | | | 6.0V | 20 | 41 | 51 | 61 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay Between Stages $Q_n$ to $Q_{n+1}$ | | 2.0V | | 125 | 156 | 188 | ns |
| | | | 4.5V | | 25 | 31 | 38 | ns |
| | | | 6.0V | | 21 | 26 | 31 | ns |
| $t_{REM}$ | Minimum Reset Removal Time | | 2.0V | | 100 | 125 | 150 | ns |
| | | | 4.5V | | 20 | 25 | 30 | ns |
| | | | 6.0V | | 17 | 21 | 25 | ns |
| $t_W$ | Minimum Pulse Width | | 2.0V | | 80 | 100 | 120 | ns |
| | | | 4.5V | | 16 | 20 | 24 | ns |
| | | | 6.0V | | 14 | 17 | 20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Time | | 2.0V | | 1000 | 1000 | 1000 | ns |
| | | | 4.5V | | 500 | 500 | 500 | ns |
| | | | 6.0V | | 400 | 400 | 400 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 10 | 15 | 19 | 22 | ns |
| | | | 6.0V | 9 | 13 | 16 | 19 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | (per package) | | 55 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

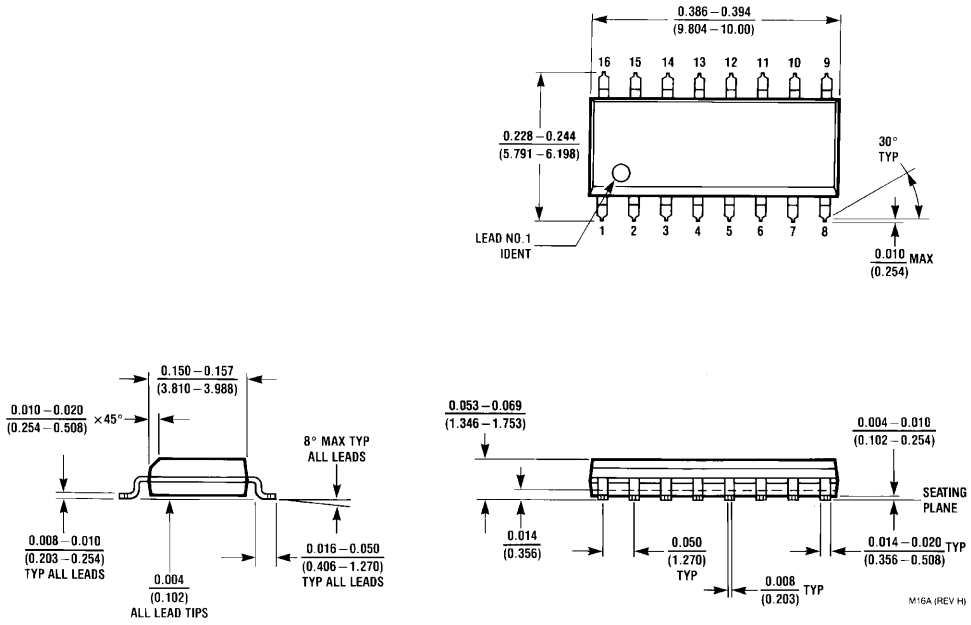
**Note 5:** Typical Propagation delay time to any output can be calculated using: $t_P$ = 17+12(N–1) ns; where N is the number of the output, $Q_W$, at $V_{CC}$ = 5V.

**Note 6:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

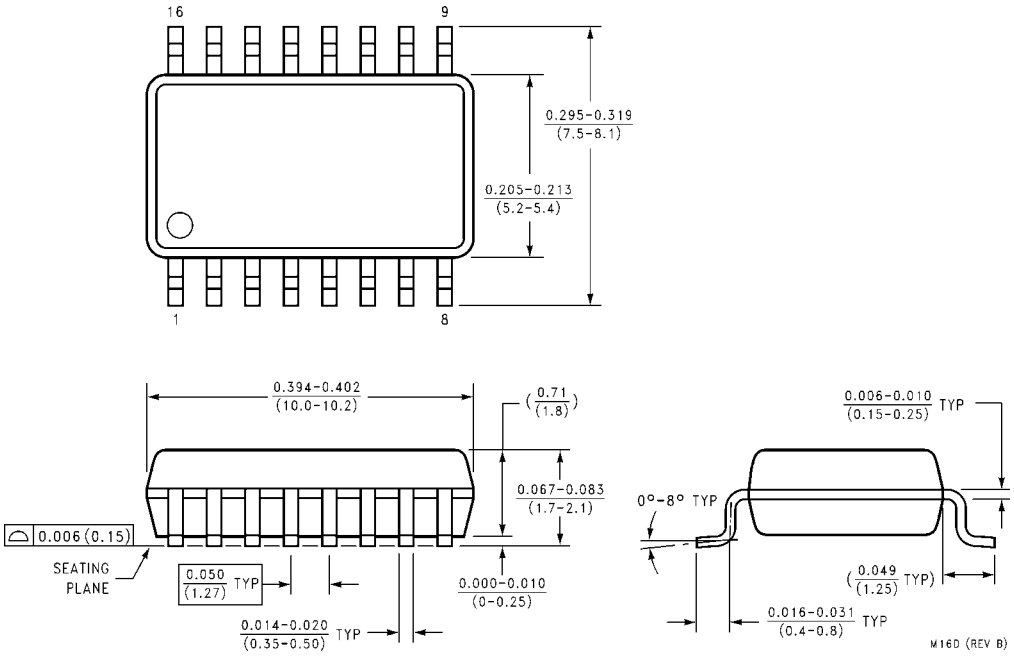
## Timing Diagram



## Physical Dimensions inches (millimeters) unless otherwise noted

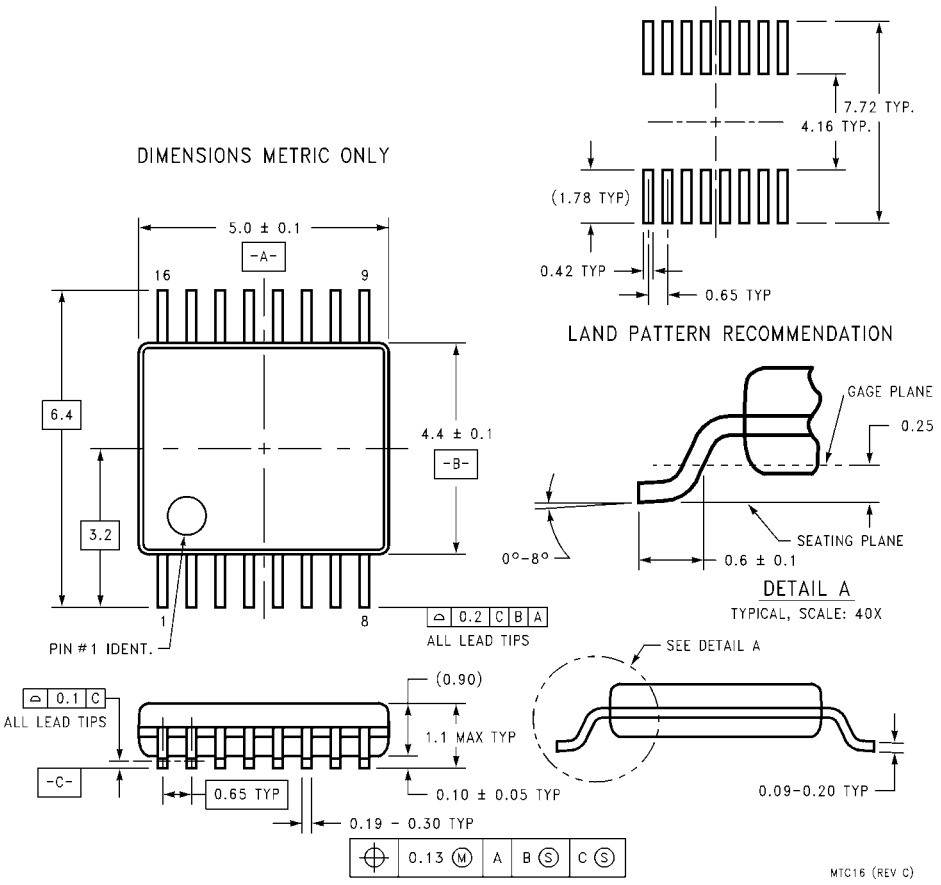



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**



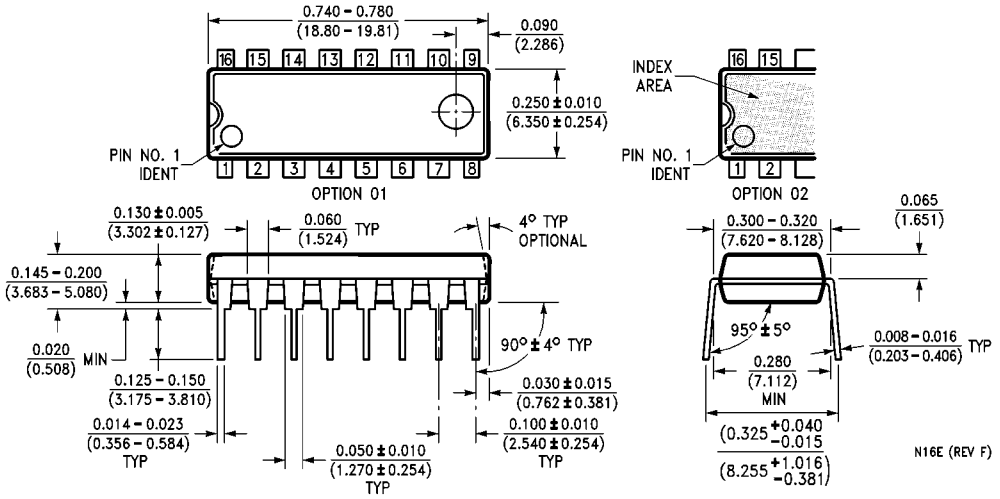

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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